Reducing Defective Alignment of Laser Drilling Process

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Abstract. The manufacturing process of multi-layer printed circuit boards (PCBs) includes repeated etching, lamination, drilling, plating, and coating processes. The substrate of PCBs may expand or contract after the lamination process. A stack of substrates with a high variation in the thermal expansion rate would cause poor alignment in the following laser drilling process. This phenomenon may even cause electrical short or open. The goal of this research is to reduce defective alignment of the laser drilling process by minimizing the variation of the thermal expansion rate of substrates. Three critical parameters were investigated: prepreg material, position of the register mark, and the number of product boards per stack of the lamination process. Full factorial design at two levels was applied for analysis. After implementing the parameter setting suggested by this research, the investigated PCB fabricator decreased defective alignment of the laser drilling process from 4.90% to 1.31%. This improvement saved the production cost around 16 million Taiwan Dollars per year, which was significant.

Keywords: process variation, quality engineering, printed circuit boards

1. INTRODUCTION

Printed circuit boards (PCBs) are widely used in electronic products. Electronic components are connected together, by soldering to PCBs, to create an electronic circuit with certain functions. This research investigate the quality of the manufacturing process of multi-layer PCBs which have a higher component density than single or double sided PCBs have. The manufacturing process of multi-layer PCBs includes repeated etching, lamination, drilling, plating, and coating processes. The lamination process is one of the key processes to making qualified multi-layer PCBs. (Coombs and Holden, 2016). Several multi-layer boards are often laminated in a stack for the productivity purpose. However, each board in a stack may have different level of dimensional changes due to the distribution of pressure and heat applied on the boards during lamination. To ensure the integrity of multi-layer boards, each step of the manufacturing process has to ensure accurate registration.

Multi-layer boards go through the drilling process after the lamination process. The locator holes for the drilling process are obtained by milling and drilling the registration marks on the inner layers of PCBs. Khandpur (2005) pointed out that the probability of mis-registration increases dramatically as the number of layers increases or pad sizes decrease. Hinton (1992) discussed various methods for solving the problems of internal layer registration in multi-layer boards. Recently, Automatic Optical Inspection (AOI) is the popular method used for accurate inspections in the PCB fabrication industry, as in Singh and Bharti (2012) and Kim *et al.* (2016).

Watanabe *et al.* (2008) studied the impact of rotational speed and the radio run-out of drills on hole quality of PCBs. Zheng *et al.* (2012) also pointed out that the feed rate, spindle speed, and tool wear would affect hole quality. Suganthi *et al.* (2015) reviewed the micro-drilling techniques and strategies that were adopted to improve the accuracy in holes. In the drilling process, scaling PCBs is required to compensate for substrate expansion during lamination. (Tavernier, 2015) In the case study of this research, the PCB fabricator applies AOI and the average thermal expansion rate to compensate for substrate expansion at different workstations of laser drilling. This research focuses on solving the alignment problem at the workstations that uses the average thermal expansion rate

for compensation. Notably, the thermal expansion rate of each board in a stack differs. Applying the average thermal expansion rate for board scaling may cause poor alignment during the laser drilling process. Holes may be drilled at inaccurate positions, which could lead to electrical short or open. Thus, reducing the variation of the thermal expansion rate during lamination is influential to improving the alignment of the laser drilling process and producing qualified PCBs.

The lamination process inevitably introduces fabrication deviation or layer distortion. The goal of this research is to reduce dimensional variation of PCBs during the lamination process to achieve precise alignment in the laser drilling process. In Section 2, the calculation of the thermal expansion rate used by the investigated PCB fabricator is explained. Section 3 introduces the procedure that identifies the critical factors to substrate expansion, analyzes the best level combination of these factors to minimize the variation of the thermal expansion rate in a stack of product boards, and validates the results. Section 4 presents a cases study of multi-layer PCB fabricator. Section 5 concludes this research with discussions.

2. THERMAL EXPANSION RATE

In the lamination process, multi-layer boards are subjected to heat and pressure to encapsulate the circuits and fill any buried via. Several materials are joined together by prepreg materials to achieve the designed number of layers and thickness of a board.

Figure 1 illustrates an example of the substrate expansion of a multi-layer board. Let CLT, CLB, CRT and CRB be the register marks of the original product set by Computer Aided Manufacturing (CAD). Let LT, LB, RT, and RB be the register marks captured by machines after the lamination process. The characters C, L, R, T, B stand for CAD, left, right, top, bottom, respectively. Let *m1*, *m2*, *n1*, *n2*, *x1*, *x2*, *y1*, and *y2* be the Euclidean distance between the aforementioned register marks as shown in Figure 1.

The lamination process may cause different level of distortion on the four sides of a product board. To calculate the dimensional expansion in the x axis, the average distance between the left and the right register marks captured by machines is compared with the average distance between the left and the right register marks set by CAD. Similarly, the average distance between the bottom and the top register marks captured by machines is compared with the average distance between the bottom and the top register marks set by CAD to calculate the dimensional expansion rate in y axis. For simple usage in the PCB industry, the investigated PCB fabricator defines the thermal expansion rate of a substrate in the x and y axes, d_x and d_y, as follows.

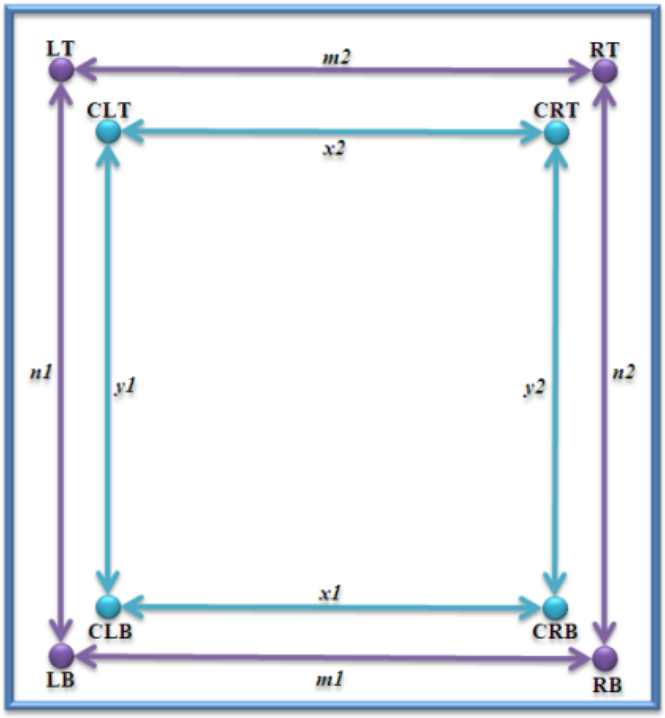


Figure 1: The illustration of register marks.

$$d_x = \frac{(m1+m2)/2}{(x1+x2)/2} \times 100\% , \quad (1)$$

$$d_y = \frac{(n1+n2)/2}{(y1+y2)/2} \times 100\% . \quad (2)$$

Having a rate greater than one indicates substrate expansion, whereas having a rate less than one indicates substrate contraction.

3. METHODOLOGY

3.1 Cause Effect Analysis

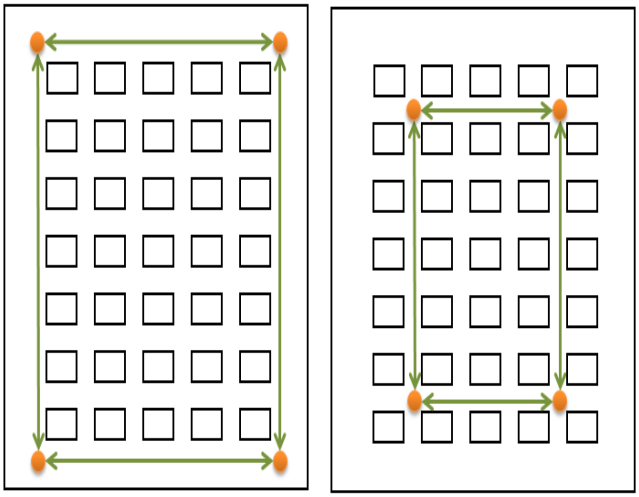
After the lamination process, the thermal expansion rates of several sampled boards are calculated as in (1) and (2). The investigated PCB fabricator in this study then uses the average thermal expansion rate from the samples to scale the boards in a stack for the laser drilling process. If the expansion rate of each board is similar, the laser drilling process could better hit the target on copper pads. On the contrary, having highly varied expansion rates could cause poor alignment shifted away from the center of a target.

The proposed methodology firstly applies the cause and effect analysis to determine the potential factors to having a large variance in the thermal expansion rate during lamination. The PCB fabricator in this study had started several projects to solve certain factors. For example, the

fabricator set the standard operation procedure to avoid operators making mistakes; increased the frequency of machine maintenance to improve machine capability, and increased the frequency of raw material sampling to improve production quality. This research then focused on the parameters of the lamination and drilling processes. After discussing with senior engineers and managers of the investigated PCB fabricator, three factors were studied in this research A: prepreg material, B: position of register mark, and C: number of product boards per stack during lamination.

Prepreg is one of the main materials to multi-layer PCBs. Resin content, resin flow, gel time, volatile content are key performance indicators of prepreg materials. For example, the prepreg material with low fluidity tends to cause bubbles or fails in filling gaps graphics. Resin content is influential to the dimensional stability of PCB substrates, too. Thus, selecting a prepreg material is important to controlling substrate expansion. The investigated PCB fabricator considered to apply a new material in the lamination process. The new material requires less processing time of lamination, and may decrease the variance of the thermal expansion rate of a substrate.

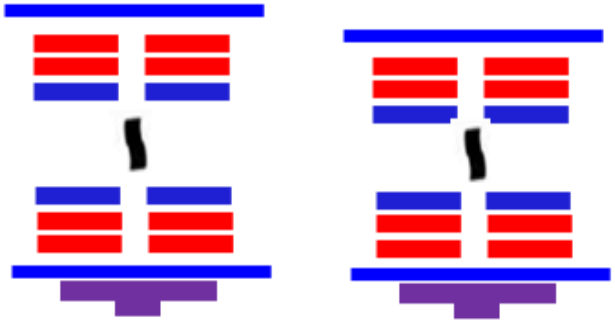
During the lamination process, the temperature and pressure near the center of a board is more stable than that around the edges of a board. The thermal expansion rate is more varied if setting the register marks at the outer part of boards. Therefore, this research considered moving the register marks inside by one grid as shown in Figure 2.



(a) (b)

Figure 2: The illustration of the (a) outer design and (b) inner design of register marks.

The number of product boards per stack of the lay-out process may also influence the variation of the thermal expansion rate. When having fewer boards in a stack, the pressure and temperature applied to each board is more uniform. Thus, the thermal expansion rate of each board may be closer. The investigated PCB fabricator in this research sequentially processes 180 product boards per lot. For productivity reason, the number of product boards per stack should be a multiple of 3, say 15, 12, 9, …, during lamination. However, reducing the number of product boards per stack would decrease production capability. Thus, this case study investigated reducing from the current setting of 15 layers per stack to 12 layers as illustrated in Figure 3.



(a) (b)

Figure 3: The illustration of the number of product boards per stack, (a) 15 layers (b) 12 layers.

3.2 Data Collection

In this research, full factorial design at two levels is applied to find the best setting with the smallest variation in the thermal expansion rate of PCB substrates. Table 1 lists the three investigated factors and their levels. The 2^3 design with 8 runs is applied as shown in Table 2. The thermal expansion rate of ten samples are collected under each of the 8 runs. Denote $d_{x,i,j}$ and $d_{y,i,j}$ as the thermal expansion rate of the jth sample under the ith run in the x and y axis, respectively, i = 1, 2, …, 8, j = 1, 2, …, 10. Let $s^2_{x,i}$ and $s^2_{y,i}$ be the sample variance of the 10 thermal expansion rates under the ith run in the x and y axis, respectively, i = 1, 2, …, 8.

Table 1: The level of the analyzed factors.

Factor	Explanation	Level (-1)	Level (1)
A	prepreg material	New	Current
B	position of register mark	inner design	outer design
C	number of product boards per stack	12	15

Table 2: The design matrix.

Run i	A	B	C
1	-1	-1	1
2	-1	1	1
3	1	1	-1
4	-1	-1	-1
5	-1	1	-1
6	1	-1	-1
7	1	1	1
8	1	-1	1

3.3 Analysis

The impact of the three factors on the variation of the thermal expansion rate may differ in x and y axes. Thus, the rates of the two axes are separately analyzed. The objective is the find the best level combination of the three factors that minimizes the variation in both axes after lamination. To measure the dispersion effects of factors, the sample variances can be analyzed by taking the nature logarithm transformation. (Wu and Hamada, 2009) Denote $\ln s_{x,i}^2$ and $\ln s_{y,i}^2$ as the transformed sample variances of the ith run in the x and y axes, separately, i = 1, 2, …, 8. The transformed sample variances are treated as the responses under each run. Then, the standard analysis of factor effects on mean can be applied based on the transformed sample variances.

The main effects and interaction effects based on $\ln s_{x,i}^2$ and $\ln s_{y,i}^2$ are plotted. Then, the half-normal plots are used for testing effect significance. Any factor lying away from the reference straight line is considered as significant.

After identifying significant factors, regress $\ln s_{x,i}^2$ and $\ln s_{y,i}^2$ on the significant factors by the least-squares method. The expected variance of thermal expansion rate can be calculated by plug-in the best combination of the levels leading to the minimum data dispersion. Lastly, repeat the lamination process for N times and calculate the average thermal expansion rates for validation under the best combination of the levels.

4. NUMERICAL RESULTS AND DISCUSSIONS

The analysis results on both x and y axes were similar. The following research presents the numerical results of data dispersion on the x axis only for simplicity. The main effects plots in Figure 4 suggested that choosing the level of -1 for all the three factors could lead to a low variation in the thermal expansion rate. Furthermore, there was no interaction among the three factors as shown in Figure 5. The dashed line at level 1 did not cross with the straight line at level -1. The half-normal plot in Figure 6 suggested that only the three main effects were significant, whereas the two-factor or three-factor interaction effects were insignificant. The fitted regression model was $\ln \sigma_x^2$ = - 4.368 + 0.100A + 0.118B + 0.169C with a R-square of 98.46%; $\ln \sigma_y^2$ = - 4.283 + 0.099A + 0.122B + 0.155C with a R-square of 98.51%. The impact of the three factors on the variation of substrate expansion were similar in both x and y axes.

In summary, the analysis suggested that replacing the prepreg material with the new material, moving the position of register marks toward the center of the board by one grid, and reducing the number of product boards per stack from 15 to 12 layers at the lay-out process could decrease the variation of the thermal expansion rate after the lamination process. Under such combination, the expected variance of thermal expansion rate in the x and y axes are *exp*(-4.755) = 0.0086085 and *exp*(-4.659) = 0.0094759. On the contrary, the expected variance in the x and y axes are *exp*(-3.981) = 0.0186670 and *exp*(-3.907) = 0.0201007, under the current setting used by the investigated PCB fabricator, respectively. The new setting may bring the variance to around 46% of the current variance.

This study repeated the lamination process under the best setting for N = 10 times. The average variance of the thermal expansion rate in the x and y axes were *exp*(-4.804) = 0.0081969 and *exp*(-4.771) = 0.0084719, respectively, which were very close to the expected values. The investigated PCB fabricator of this research implemented the best setting and brought down the defective rate of the laser drilling process from 4.9% to 1.31%. This improvement saved the production cost around 16 million Taiwan Dollars per year, which was significant.

5. CONCLUSIONS

The lamination process is influential to the alignment of the following laser drilling process. PCB substrates may have different level of dimensional change after lamination. If the thermal expansion rate greatly varied from board to board, using the average expansion rate to compensate dimensional change would cause defective holes in the laser drilling process. Thus, this research used the full factorial design at two levels to investigate the best setting that can minimize the variance of expansion rates. The validation experiment also confirmed the contribution of changing the current setting to the best setting suggested by this research.

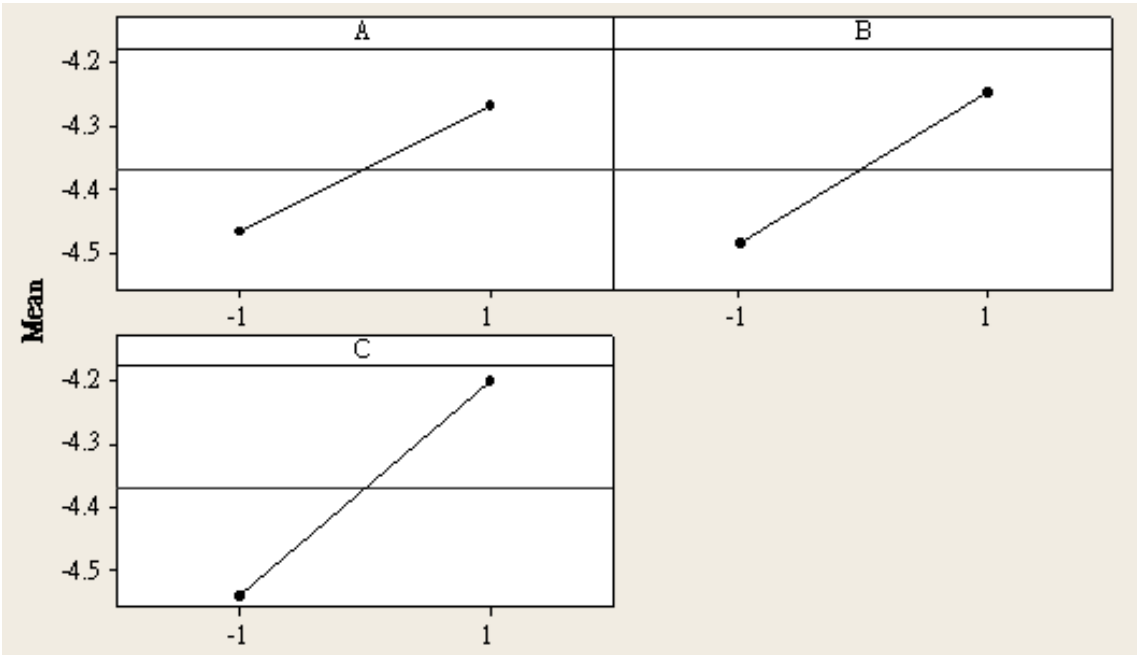


Figure 4: The main effects plots of data dispersion.

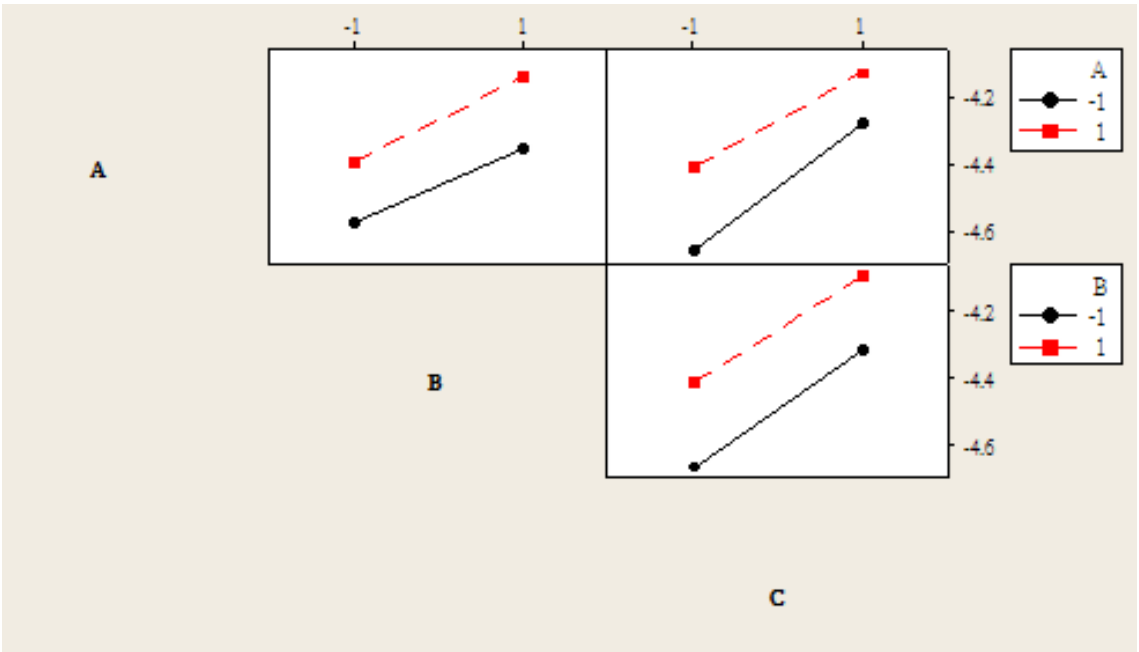


Figure 5: The interaction effects plots of data dispersion.

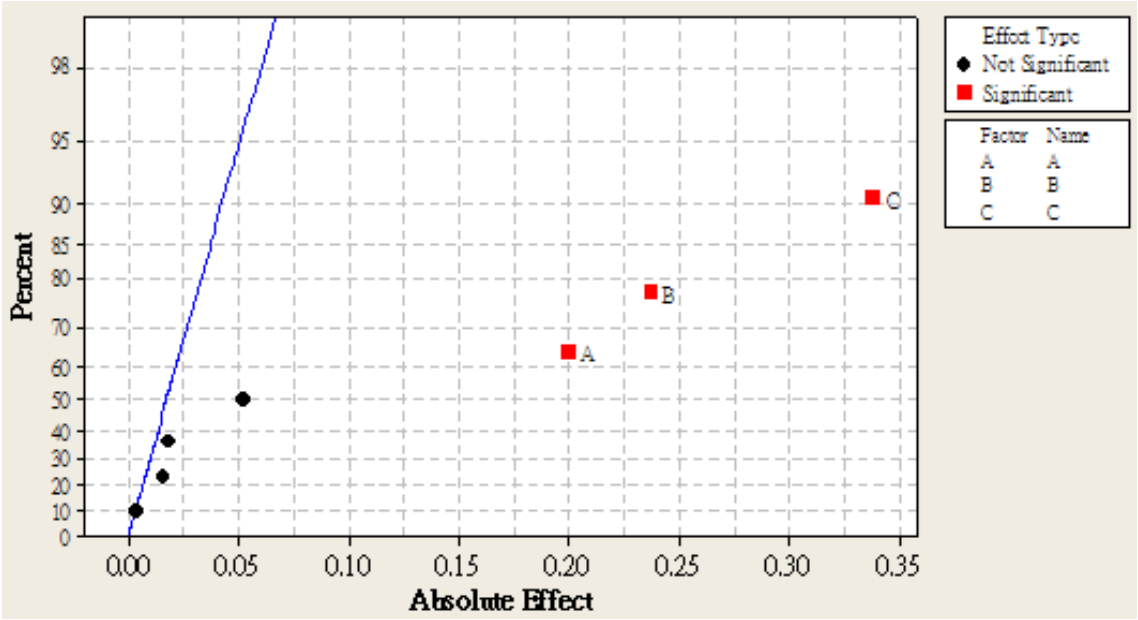


Figure 6: The half-normal plot of data dispersion.

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